Gate Controlled Diodes for Characterization of the Si-SiO_2 Interface with Respect to Surface Effects of Silicon Detectors

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Abstract

In future high energy physics experiments silicon detectors with a high spatial resolution will be used for tracking close to the interaction point. Besides crystal damage, the surface damage caused by ionizing irradiation is very important for the long term performance of these devices. Therefore systematic characterization of surface effects is necessary. For these investigations we designed a test field consistent of MOS structures and gate controlled diodes to be produced with different vendors. A new gate controlled diode with different current and capacitance measurement options will be introduced and first results of parameters evaluated on the unirradiated device as well as after irradiation with low energetic electrons, neutrons and charged hadrons will be presented. The gate controlled diode with new features has been shown to be a powerful tool to investigate the oxide and interface quality before and after irradiation.

Key words: gate controlled diode, interface state density, interface generation current, oxide charge, silicon detector, surface damage

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1 Introduction

Silicon detectors are often used where a high spatial resolution is required. This is especially the case for future high energy physics experiments e.g. in tracking regions close to the interaction point where the two track resolution

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needs to be high and secondary vertices have to be resolved. In these locations the highly segmented detectors will encounter a very harsh radiation field, dominated by charged hadrons. As pointed out in general radiation damage studies (see e.g. (1)), it is necessary to study the surface damage as well as the bulk damage effects. For the bulk damage induced changes of the detector parameters which scale with the non-ionizing energy loss, NIEL, a parametrisation as function of flux, time and temperature has been developed, which allows a good prediction of the detector performance. Nothing comparable exists so far for the ionization induced surface effects. However, several studies have been performed showing the effects due to the ionization in the oxide layer which can also be understood qualitatively, e.g. in (2). The radiation induced increase in the oxide charge is mainly responsible for the flat-band voltage shift and the introduction of interface states which results in an increase in the interface generation current. Both effects depend on the electric field distribution during irradiation. This effect can be very pronounced (3), as it qualitatively is explained in ref. (4).

This dependence on the electric field is also one reason for the poorly understood design dependence. Lack of an appropriate model for the field dependence makes it impossible to investigate the surface damage directly on highly segmented detectors. This is especially the case, if the basic parameters, flat-band voltage and interface generation current, can not be measured with those devices, but influence the detector performance indirectly. The surface effects also depend on the applied technology and uncontrolled process variations, which determine the oxide and the interface quality.

Since surface effects have a significant influence on the tolerance to ionizing radiation, it is important to develop a set of crucial parameters which can be measured before exposure to radiation; allowing prediction of ionization induced changes quantitatively. As a first step in this direction, we designed a test field consisting of MOS structures and gate controlled diodes to be included besides the main devices in the wafer layout. This test field serves four different purposes:

- Measuring the surface parameters of individual wafers which are not measurable on the main devices, but which can be correlated with their performance and are available as input for device simulations.
- Having the identical mask layout, this structure allows comparing the technology and processing used by different vendors, especially with respect to the radiation hardness.
- Monitoring the same process dependent parameters during the production phase which allows identification of possible processing problems before detectors are built into modules. An essential step in this direction will be to evaluate the crucial parameters.

- Systematic studies of ionization induced radiation damage including the process dependent parameters and the electric field conditions during irradiation. The target is to develop a set of ionization dose dependent input parameters for device simulation which allows the prediction of surface damage effects for any design.

In the following section, we introduce a new gate controlled diode configuration which will allow special measurements and measurement conditions not possible with standard gate controlled diodes. Following this, the different measurable characteristic parameters will be introduced and the first exemplary results will be presented.

2 Design of the advanced gate controlled diode

The test field was designed for the p^+-side and implemented in the mask layout designed for the ROSE collaboration (5). This mask set also includes several test diodes; mainly for investigations of bulk damage. The layout for the test field is also available for the n^+-side with p-stop (6) and with p-spray (7) isolation technique. All three versions have been included in the wafer layout of the first ATLAS pixel sensor prototype on n-bulk silicon (8). Several silicon detector design groups and vendors of silicon detectors received the complete layout files in GDS-II format by now and have included this test field in their mask layout [2].

The test field is shown in Figure 1 and consists of two circular MOS structures and two advanced gate controlled diodes. The advantage of this redundancy is to have either always an identical reference sample or to have the possibility to irradiate two identical samples under different electrical boundary conditions.

The gate controlled diode is formed by a $7.9 \cdot 10^{-3}$ cm^2 circular diode which is surrounded by 5 individual gate rings each 50 μm wide with 5 μm gaps. There are several advantages to have more than one gate ring as it was the case up to now for the standard gate controlled diode which was first introduced in ref. (9) and often used in semiconductor technology. It is possible to define the lateral extension of the contributing depletion zone by keeping the outer gates in accumulation. Also several gates can be connected together to build a larger gate contact. This for example is important for studies on the interface generation current or on the dependency of effects on the lateral distance to the diode. Furthermore each gate can be characterized individually using C-V measurements with a well defined area. Any influence of the neighbor gates can be eliminated by keeping them in accumulation. This allows to measure

[2] GDS-II files for the test fields are available on request from the authors.

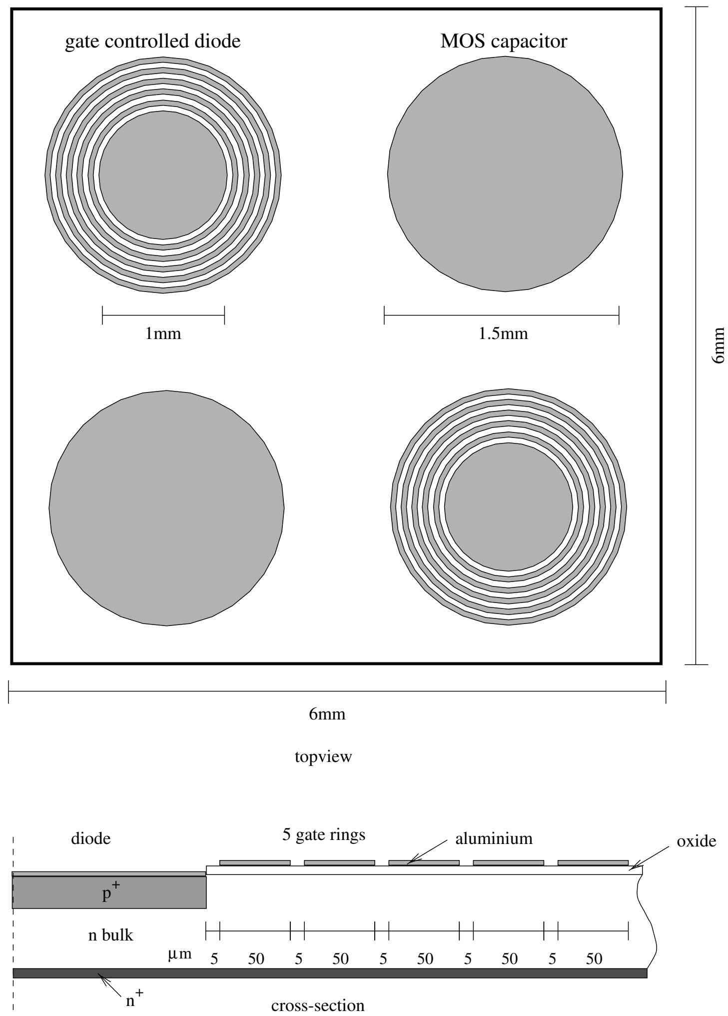

Fig. 1. Top-view and cross-section of the test field.

the density of positive oxide charges and the interface generation current (see section 3) on the identical device. Thinking of irradiation tests, it is of interest to adjust individual potentials to the rings during irradiation.

The circular MOS capacitors have a gate area of $17.7 \cdot 10^{-3}$ cm^2. They are very useful to determine the flat-band voltage and the oxide capacity per unit area.

3 Introduction of characteristic parameters

The most often discussed parameter in connection with MOS devices is the flat-band voltage V_{fb}. It describes the potential which has to be adjusted to the MOS device to flatten the energy bands. It is a direct measure for the concentration of positive oxide charges N_{ox} trapped in the oxide,

$$\Delta V_{fb} = \frac{q_0 d}{\epsilon_0 \epsilon_{ox}} \cdot \Delta N_{ox}, \tag{1}$$

where d represents the oxide thickness, q_0 the electron charge, ϵ_0 the dielectric constant and ϵ_{ox} the permittivity of the oxide. Further details can be found for example in (10).

The interface generation current is caused by generation of charge carriers in the interface,

$$I_{ox} = q_0 n_i S_0 A_{gate}, \tag{2}$$

where n_i is the intrinsic charge carrier concentration, A_{gate} the gate area and S_0 the interface recombination velocity. S_0 is given as

$$S_0 = \sigma v_{th} \pi k_B T D_{it}, \tag{3}$$

with σ being the effective capture cross-section of the interface trapping centers, v_{th} the thermal velocity of the minority carriers, k_B the Boltzmann constant, T the absolute temperature and D_{it} the interface state density in $\mathrm{cm^{-2}eV^{-1}}$ (9).

As introduced in (9) the bias voltage V_{bias} of the diode influences the shape of the energy bands of the nearby gates. For this reason the starting voltage for the formation of an inversion layer underneath the gates, called V_{inv}, is influenced by the reverse bias of the diode,

$$V_{inv} = -2q_0\phi_F + V_{fb} + V_{bias}, \tag{4}$$

where ϕ_F represents the Fermi potential.

4 Measurement of interface generation current

For determination of interface generation current I_{ox} with a gate controlled diode a fixed reverse diode bias voltage V_{bias} is applied and the current is measured as a function of the gate voltage V_{gate}. The theoretically expected I_{ox} curve is shown in Figure 2.

While the region under the gate ring is in accumulation only volume generation current I_{jd} coming from the pn-junction is observed. When V_{gate} reaches

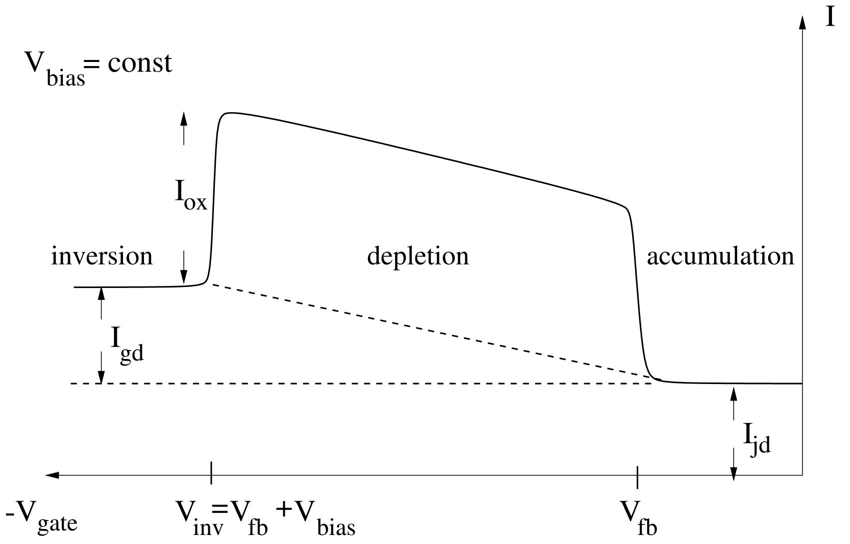

Fig. 2. *Current contributions of a gate controlled diode as a function of the gate voltage, adopted from (9).*

the flat-band voltage of the gate ring, a depletion region under the gate ring is formed which connects to the depletion region of the diode. Now in addition the generation–recombination–centers at the Si-SiO_2 interface contribute to the total current, visible as a sharp increase. Furthermore the bulk generation current of the depleted area under the gate ring, which grows with increasing gate voltage V_{gate}, contributes to the measured current. At the inversion voltage an inversion layer under the oxide is formed screening the contribution of the interface generation current. For gate voltages more negative than the inversion voltage the total generation current remains constant because the gate depletion region is pinned to its maximum depth.

In Figure 3 a set of I_{ox} curves is shown in which the current is plotted versus the gate voltage attached to the innermost gate ring while accumulating the others. The different curves belong to different reverse bias voltages of the diode. Comparing the measured results with Figure 2 good agreement is found.

Once I_{ox} is known, S_0 and D_{it} can be calculated according to equations 2 and 3. Examples of these parameters are listed in Table 1. Encouraged by the good performance of the enhanced gate controlled diode and the presented results, detailed studies on the influence of radiation damage and the variation of the interface parameters with different vendors have started.

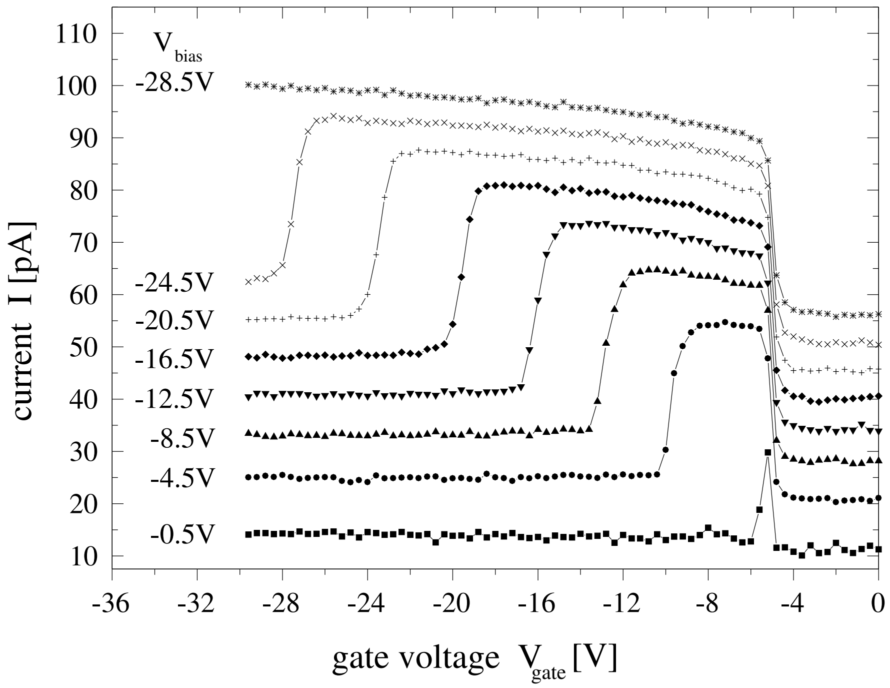

Fig. 3. *I_{ox} measurement as a function of the reverse bias applied to the diode.*

Table 1

Examples of surface parameters evaluated with gate controlled diodes; parameters for S_0 and D_{it} were derived from I_{ox} using $\sigma = 2.5 \cdot 10^{-16} cm^2$, $v_{th} = 2.0 \cdot 10^7 cm/s$, $T = 293K$ and $n_i = 7.721 \cdot 10^9 cm^{-3}$; d_{ox} was derived from C_{ox}; V_{fb} was derived from the turning point of measured C-V curves.

sample	vendor	crystal	d_{ox} $[nm]$	V_{fb} $[V]$	I_{ox}/A_{gate} $[\frac{nA}{cm^2}]$	N_{ox} $\left[\frac{10^{11}}{cm^2}\right]$	S_0 $[\frac{cm}{s}]$	D_{it} $\left[\frac{10^9}{cm^2 eV}\right]$
A	V1	<111>	885	4.0	3.8	0.8	3.0	7.7
B	V2	<100>	400	0.1	6.6	< 0.2	5.3	13.4
C	V3	<111>	175	3.0	4.8	2.7	3.8	9.7
D	V3	<111>	180	4.6	18.1	3.9	14.6	36.8

5 Capacitance measurements

A furthermore advantage of the multiple rings is the possibility to also apply capacitance methods to them. This cannot be realized with only one gate ring which always interferes with the diode. The influence of the neighborhood of an individual ring is shown in Figure 4. The curves which were obtained with the inner neighbors floating show an increase of capacitance in case of strong inversion. It is not observable when the inner gates are kept in accumulation. The explanation for this behavior is that the p–conducting inversion layer

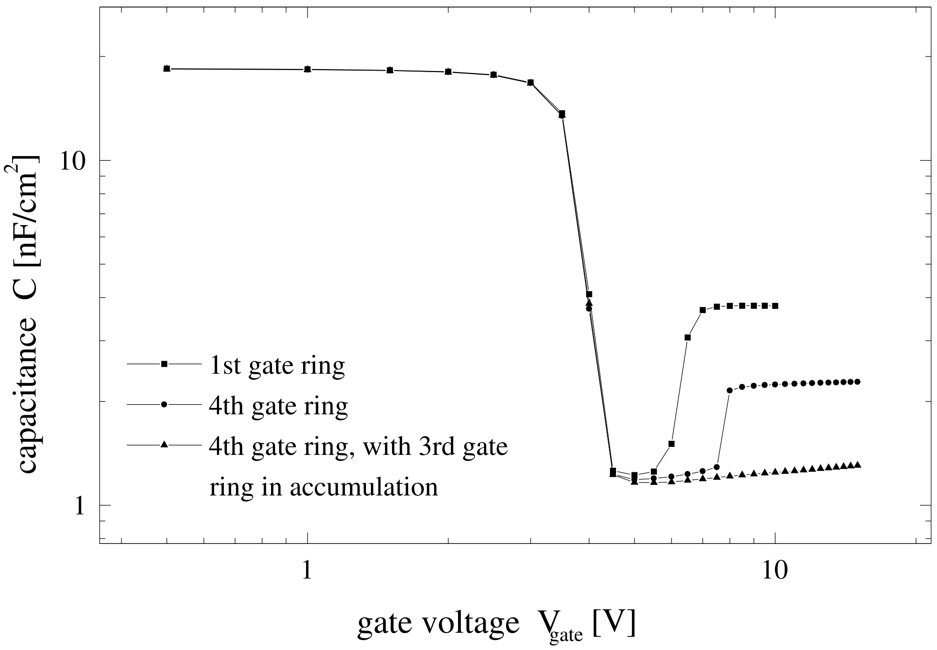

Fig. 4. *High frequency C-V curves of gate rings of sample D (ν=10 kHz, V_{lvl}=50 mV).*

underneath the inverted gate merges with the p^+–doped region of the diode. Therefore a charge exchange with the p^+–doped region is possible which contributes even to the high frequency C-V characteristics. The charge exchange can be suppressed by accumulating the gate area between the measured ring and the diode.

A common method to measure the interface state density D_{it} on MOS structures is the combined high–low frequency capacitance method (11). In case of depletion interface trap occupancy changes by capture and emission of majority carriers. Minority carrier capture is unimportant because the minority carrier density is very low. In a high frequency measurement the interface traps cannot respond to the signal but using a low frequency measurement the interface trap response is prompt. Therefore, an additional capacitance C_{it} contributes to the measured low frequency C-V curve. Accordingly D_{it} can be expressed as

$$D_{it} = \frac{C_{it}}{q_0} = \frac{C_{LF} - C_{HF}}{q_0} \left(1 - \frac{C_{LF}}{C_{ox}}\right)^{-1} \left(1 - \frac{C_{HF}}{C_{ox}}\right)^{-1}, \qquad (5)$$

with C_{LF} the value of the low frequency measurement, C_{HF} the value of the high frequency measurement and C_{ox} the oxide capacitance (11).

An example of C_{LF} and C_{HF} versus V_{gate} is shown in Figure 5. According to equation 5 the density of interface states has been calculated from the data and is plotted in the insert of Figure 5, giving an average interface state density of $D_{it} = (8.0 \pm 0.7) \cdot 10^9$ cm^{-2}eV^{-1}. If one compares this value with the result obtained from the I_{ox} measurements, $D_{it} = (7.7 \pm 0.3) \cdot 10^9$ cm^{-2}eV^{-1}, good agreement is found. Therefore, the advanced gate controlled diode features two independent methods for determining the interface state density.

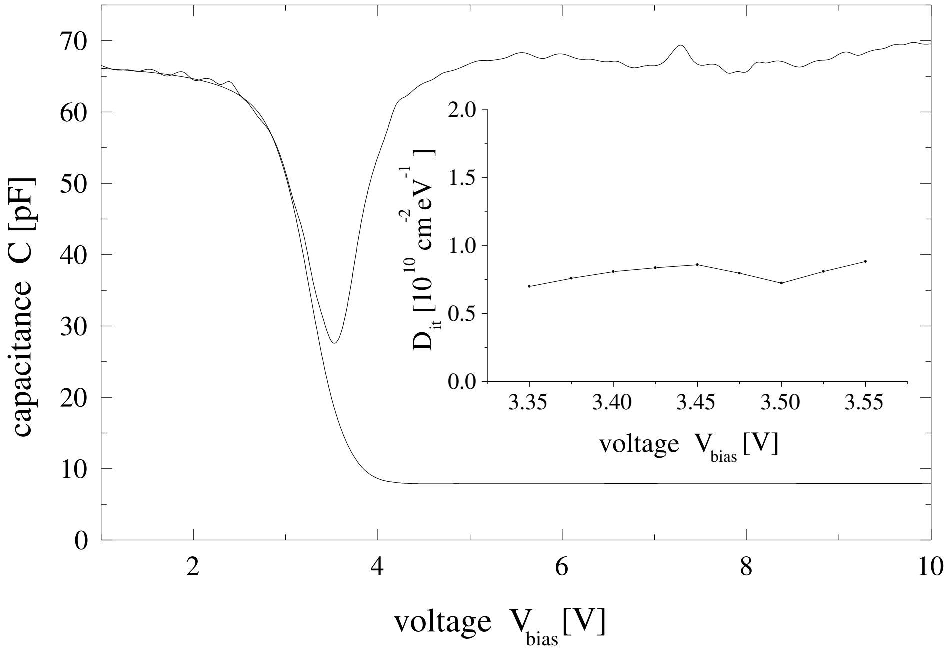

Fig. 5. *High frequency (*10 kHz*) and low frequency (*0.5 Hz*) C-V curves for a MOS capacitor of sample A. The resulting interface state density from equation 5 is shown in the insert.*

6 Measurements after electron irradiation

To study the effects of ionization induced radiation damage C-V characteristics of gate rings and I_{ox} curves of a gate controlled diode were measured before irradiation and after exposure to several dose levels. All measurements were made 24 hours after irradiation, keeping the temperature at (20 ± 1)°C until the next irradiation. Although the exact time and temperature dependence of the annealing is not known yet, this allows to compare the results. Detailed studies of the annealing behavior of surface damage have started. For all irradiations an electron beam of 20 keV at the Dortmund Irradiation Facility (12) was used and no bias was applied to the structure. The dependence of the surface damage induced from the bias voltage applied during irradiation is currently under study. Also this study will benefit from the gate controlled diode with multiple gate rings as they allow to study different distributions of the electric field.

A set of high frequency C-V curves before irradiation and after exposure to several dose levels is shown in Fig. 6. After exposure to ionizing radiation, the transition region of the C-V curves is stretched out along the voltage axis. This voltage stretch-out can be explained by an increase in the interface trap level density. In addition to the stretch–out, the shift of the C-V curve has been altered. The V_{fb} shift along the voltage axis of the C-V curves to more negative voltages indicates that positive charge is induced in the oxide as a result of the ionizing radiation.

Fig. 7 shows a result of I_{ox} measurements before and after irradiation. Here an obvious increase of the interface generation current with accumulated irradiation is found. Because of the shift of flat-band voltage the interface generation current contribution moves to more negative gate voltages V_{gate}. The different heights of the volume generation current I_{jd} in the accumulation case can be explained by lateral depletion around the p$^+$-implantation under the small gap of irradiated oxide between diode and inner gate ring (see Fig. 1). Therefore a permanent interface generation current of this depletion area contributes to the measured current. This was confirmed by device simulations. When the inversion voltage V_{inv} is reached the measured curves of the irradiated gate controlled diode show the expected screening of interface generation current by an inversion layer. The second increase of measured current as observed here was not seen before. The reason for this behavior is not understood yet but will be studied further.

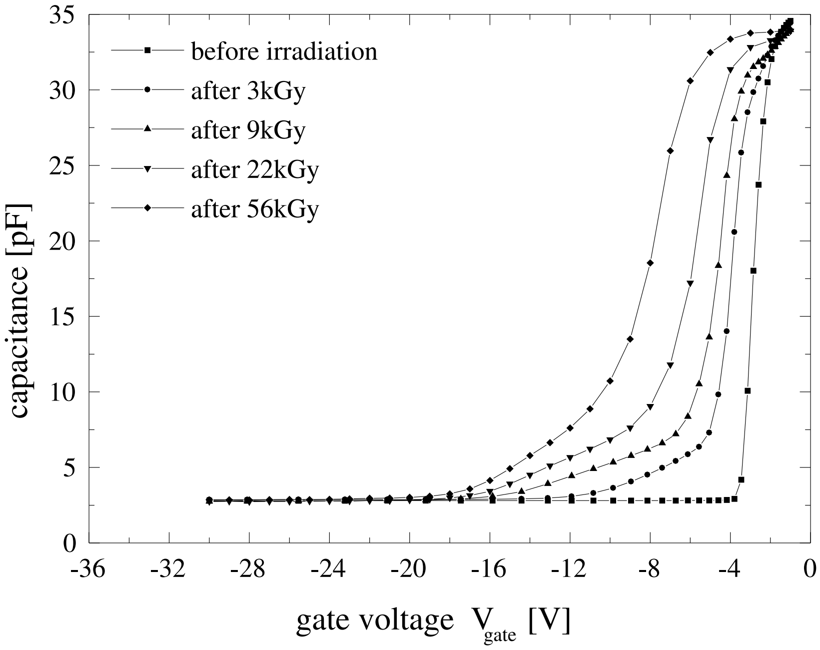

Fig. 6. *Shift along the voltage axis of gate ring C-V characteristics ($10kHz$) as a result of irradiation at several dose levels. All measurements were made on the middle gate ring with neighbor rings kept in accumulation (sample C).*

The shift of flat-band voltage and the increase of interface generation current as a function of dose rates is shown in Fig. 8. For both cases saturation has

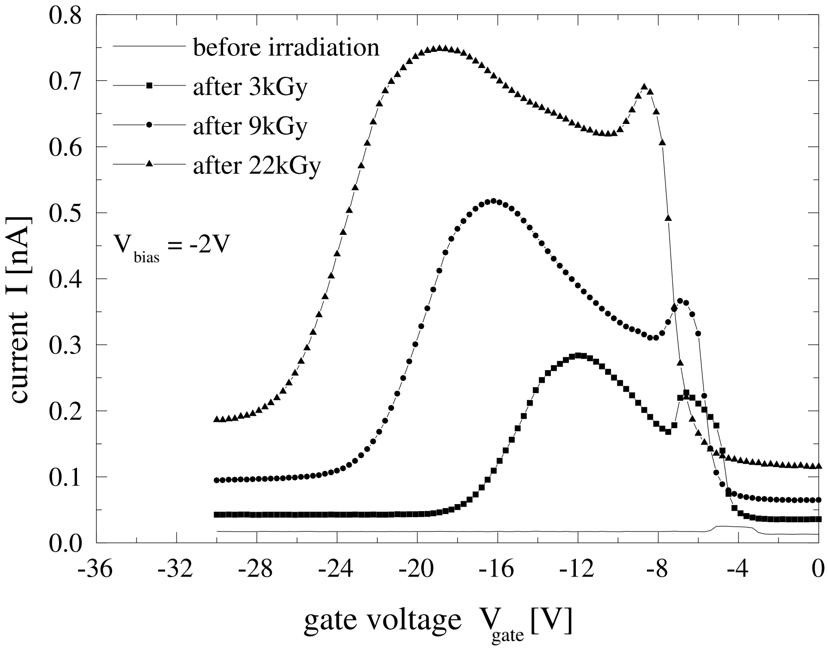

Fig. 7. *I_{ox} curves before and after irradiation with $20keV$ electrons of sample C for $V_{bias} = -2V$.*

not been reached yet and is expected for higher dose levels.

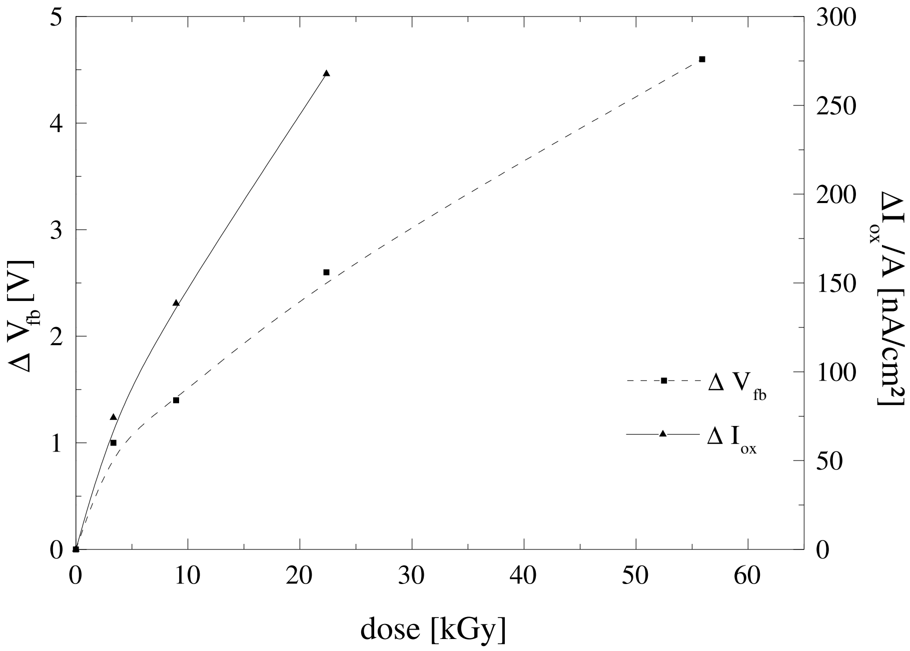

Fig. 8. *Shift of flat-band voltage V_{fb} and interface generation current I_{ox} as a function of dose (sample C).*

Table 2 summarizes some exemplary results which were obtained on the electron irradiated devices.

Table 2
Examples of surface parameters after irradiation evaluated with gate controlled diodes manufactured by one vendor; parameters for ΔS_0 and ΔD_{it} derived from ΔI_{ox} using $\sigma = 2.5 \cdot 10^{-16} cm^2$, $v_{th} = 2.0 \cdot 10^7 cm/s$, $T = 293K$ and $n_i = 7.721 \cdot 10^9 cm^{-3}$.

sample	source	$\Phi_{equ.}$ $\left[\frac{10^{13} n}{cm^2}\right]$	dose $[kGy]$	ΔV_{fb} $[V]$	ΔN_{ox} $\left[\frac{10^{11}}{cm^2}\right]$	ΔS_0 $\left[\frac{cm}{s}\right]$	ΔD_{it} $\left[\frac{10^9}{cm^2 eV}\right]$
C	electrons	n/a	3.4	1.0	1.1	60	151
C	electrons	n/a	9.0	1.4	1.5	112	282
C	electrons	n/a	22.4	2.6	2.8	216	545
E	neutrons	2.89	n/a	0	0	n/a	n/a
F	protons	2.0	11	0	0	n/a	n/a
D	protons	26	140	3.5	3.7	n/a	n/a

7 Measurements after neutron and proton irradiation

In high energy physics experiments both surface and bulk damages will be induced simultaneously. For this reason it is of interest to study the behavior of the interface region when bulk damage is present, too. This has been done by irradiating gate controlled diodes with protons. In addition to this a sample of gate controlled diodes had been irradiated with neutrons which cause bulk damage only.

Figure 9 shows an I_{ox} measurement of a neutron irradiated sample. In the plot the current of the diode measured with all gate rings in accumulation (which still includes a small I_{ox} contribution of the gap between the diode and the first ring) was subtracted from the total current.

The current curves do not show the characteristic 'current step' at the flat-band voltage and the inversion voltage which are typical for interface generation current contributions. The onsetting current increase at the flat-band voltage may not be misinterpreted as interface generation current here. What can be seen is the bulk generation current coming from the growing depth of the depletion region under the gates. When the gates start inverting, the current remains constant because the depletion zone does not grow any further.

Figures 10 and 11 show I_{ox} measurements on proton irradiated gate controlled diodes after different fluences. The current curves of the low irradiated device are of a very similar shape as that of the neutron irradiated one. The bulk generation current dominates although it is lower compared to Figure 9 due to

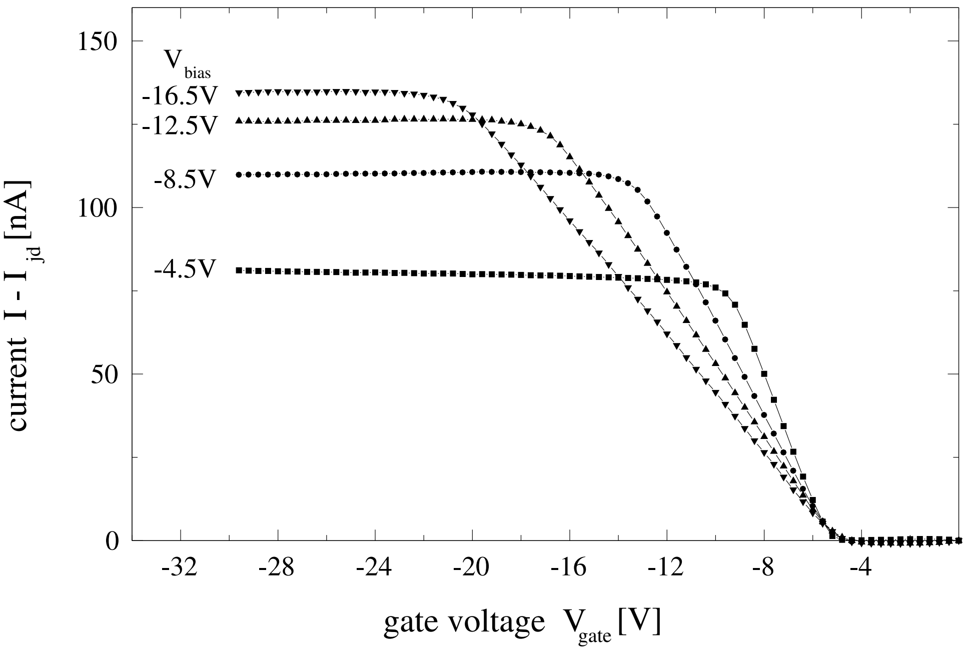

Fig. 9. *I_{ox}-curves for different diode bias voltages V_{bias} of Sample E after irradiation with neutrons ($\Phi_{equ} = 2.9 \cdot 10^{13}\ n/cm^2$).*

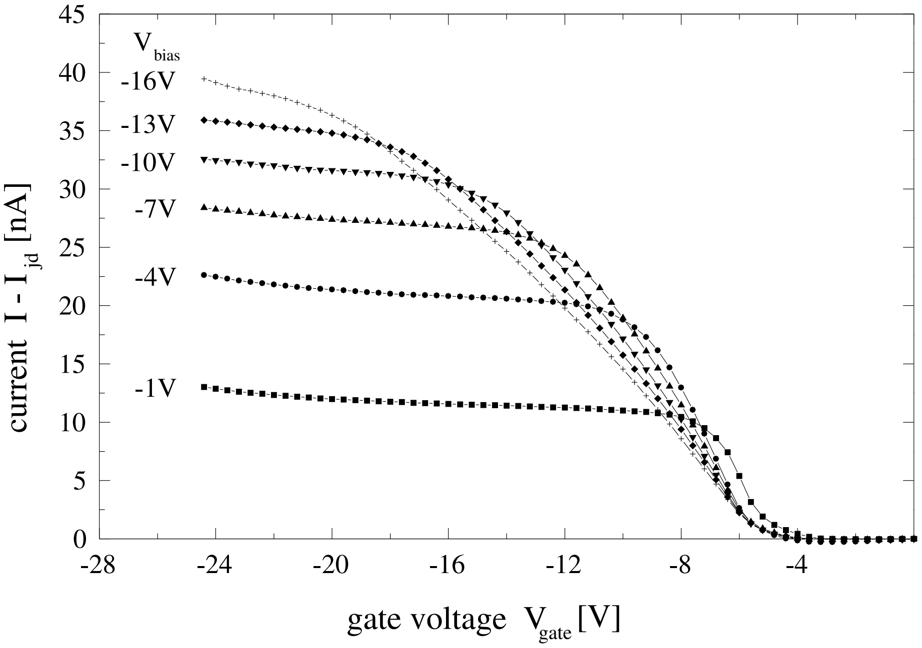

Fig. 10. *I_{ox}-curves for different diode bias voltages V_{bias} of Sample F after radiation with protons ($\Phi_{equ} = 2.0 \cdot 10^{13}\ n/cm^2$).*

a lower bulk damage. Considering the data presented in section 6 it is obvious that no interface generation current is observable because it is two orders of magnitude lower than the bulk contributions.

In case of the highly irradiated sample (Figure 11) one can observe a decrease in the flat-band voltage from -5.5 V to around -8.0 V caused by irradiation

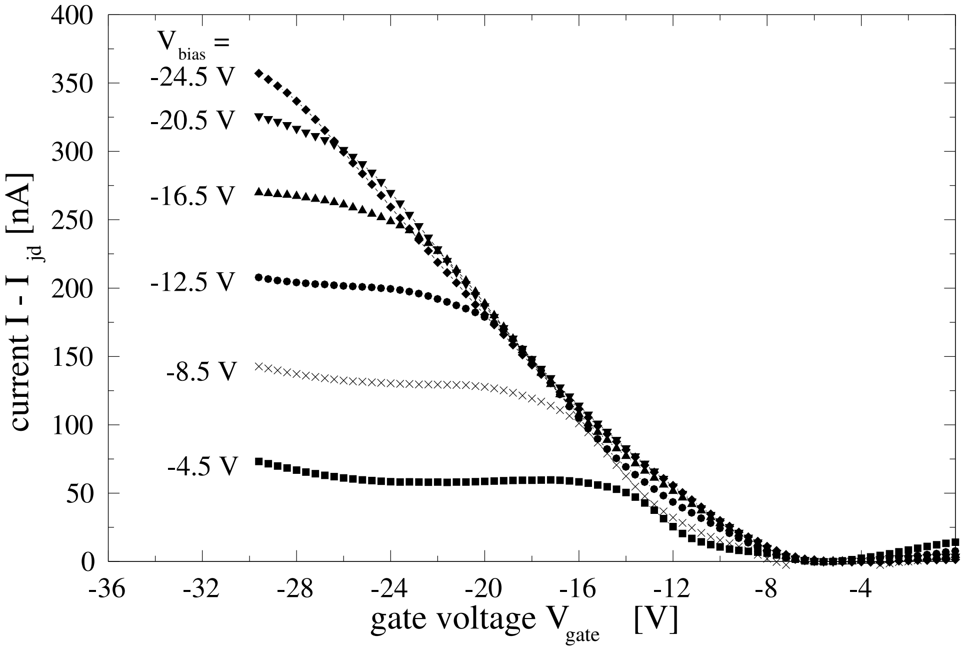

Fig. 11. *I_{ox}-curves for different diode bias voltages V_{bias} of Sample D after radiation with protons ($\Phi_{equ} = 2.6 \cdot 10^{14}$ n/cm^2).*

induced oxide charges. As expected from equation 4 the inversion voltage has decreased by irradiation correspondingly.

There is another piece of important information to be found in Fig. 11. The sample was irradiated up to an equivalent fluence of $\Phi_{equ} = 2.6 \cdot 10^{14}$ n/cm^2, which means that the bulk material has converted from n–type to p–type. If this were the case for the whole bulk, it would be impossible to deplete the regions under the gate rings at the given voltages and no additional current should be observable but it still is. Therefore, this is an indication for a remaining n–type layer located in the silicon bulk next to the interface (1). It is not possible here to estimate the depth of this layer from the data because the shape of the surface depletion region is not known.

8 Conclusions

The performance of the un-irradiated advanced gate controlled diode was found to be in good agreement with theoretical predictions. This allows to measure certain interface parameters before and after irradiation as well as vendor specific parameters which are useful for process monitoring.

The interface generation current can be measured before and after surface damage from which the interface recombination rate S_0 and the interface state density D_{it} can be determined. Alternatively it is possible to measure D_{it} with a combination of high frequency and quasi–static C-V methods. Both results have been found in good agreement. Comparing the results which were obtained on devices from different vendors and with different crystal orientations significant differences have been observed. Systematic studies on this subject have been started.

Capacitance measurements with high frequency signals on MOS devices have shown the expected shift of the flat–band voltage caused by additional oxide charges and a stretch–out of the curve after surface damage which is due to an increase of the interface state density. Current measurements on proton irradiated gate controlled diodes have shown that the interface generation current is completely negligible compared to the large increase of bulk generation current after bulk damage.

After irradiation induced type–inversion from n–type to p–type bulk material current contributions from the surface depletion zone under the gate rings are still observable without changing the sign of the gate–voltage. This is a confirmation of a remaining n–type layer in the silicon bulk underneath the interface after type inversion.

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