ROSE Technical Note

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Influence of Surface Damage on Highly Segmented Silicon Detectors

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Summary. —
Highly segmented silicon detectors have been used in high energy physics experiments already for a long time. But in future experiments they will have to survive several years in harsh radiation environments. Their performance will degenerate due to irradiation induced bulk and surface damage. Whereas bulk damage is design independent and successfully under investigation for a long time now, the design related surface damage and its consequences for a highly segmented detector are not yet well known. Therefore we have developed a test device and irradiated it systematically with low energy electrons. From I-V curves before and after irradiation we have determined the influence of surface damage on the leakage current of single pixel cells. As a main result it was found that, depending on the design, only a fraction of the surface area contributes to the interface generation current after surface damage.

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1. – Introduction

Highly segmented silicon detectors are often used for tracking and vertex finding in modern high energy physics experiments, as for example in preparation for ATLAS [1] and CMS [2]. Due to the small distance of the detectors to the interaction point, the radiation tolerance of both the silicon bulk and the surface is the most severe problem to be solved.

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Whereas bulk damage caused by non-ionising energy loss (NIEL) in the silicon crystal is already successfully under investigation for several years now as described e.g. in [3] and [4], the impact of surface damage on highly segmented detectors has not been studied in detail yet. Different to irradiation induced damage of the silicon bulk the contribution of oxide effects, as discussed e.g. in [5], is strongly correlated to the detector design.

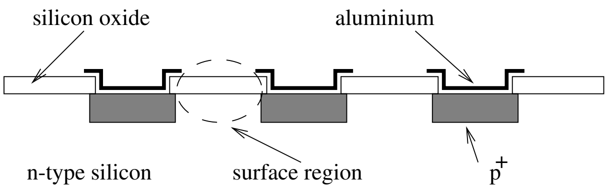

Fig. 1. – *Schematic cross–section of the segmented* p^+*-n region of a silicon detector.*

In this paper the term *surface* refers only to those regions of a device which include an interface region of SiO_2 and un-implanted silicon bulk, as indicated in fig. 1. The implanted regions are not sensitive to surface effects.

Surface effects have to be considered for designs where the size of the surface area is comparable to the size of the pn–junction. For example a "simple" pad detector has a large implanted area compared to the surface regions, therefore surface effects can be neglected. But in case of highly segmented designs like strip or pixel detectors surface effects will have to be considered as a function of the design. To be able to study this in detail it is necessary to have special test devices including systematically varied pixel designs. For our test device we have chosen the design parameters as well as integrated irradiation dose of up to 300 kGy according to the needs of high energy physics experiments.

2. – Characteristic Surface Parameters

The flat–band voltage V_{fb} which is well known from MOS–devices describes the potential which has to be adjusted to a metal–oxide–semiconductor contact to flatten the energy bands at the SiO_2–Si interface. It is a straight measure for the concentration of positive oxide charges N_{ox} trapped in the oxide and therefore sensitive to ionising radiation,

$$\Delta V_{\mathrm{fb}} = \frac{q_0 d}{\epsilon_0 \epsilon_{ox}} \cdot \Delta N_{ox}, \tag{1}$$

where d represents the oxide thickness, q_0 the electron charge, ϵ_0 the dielectric constant and ϵ_{ox} the permittivity of the oxide. Further details can be found for example in [5] and [6].

The generation of charge carriers at the interface in presence of an electric field, when the surface region is depleted, causes the interface generation current,

$$I_{ox} = q_0 n_i S_0 A_{gate}, \tag{2}$$

where n_i is the intrinsic charge carrier concentration, A_{gate} the surface area and S_0 the interface recombination velocity. S_0 is given as

$$S_0 = \sigma v_{th} k_b T D_{it}, \tag{3}$$

with σ being the effective capture cross–section of the interface trapping centres, v_{th} the thermal velocity of the minority carriers, k_b the Boltzmann constant, T the absolute temperature and D_{it} the interface state density [7]. As well as the concentration of positive oxide charges the interface state density is sensitive to ionising radiation, too.

3. – Test Device

The layout and the design of the test device have been developed at the Universität Dortmund in collaboration with the MPI in Munich [8] where the processing has been done in p^+-n-technology. High resistivity n-type float zone silicon with <111> orientation was used as substrate. The design includes all features of a detector, extended by additional test options. Fig. 2 shows a photo of the whole device of 12·12 mm^2 size. A multi guard–ring structure surrounds the pixel matrix which is divided into clusters of pixels with identical design. To achieve realistic biasing conditions in the lab and for testability reasons a *punch–through* [9] bias grid was implemented [10]. Monitor devices such as a large area diode and two MOS capacitors for measurements of global bulk and surface parameters have been included (at the bottom of fig. 2).

All pixels have got an aluminium dc contact to the p^+ implantation. The aluminium contact is slightly smaller than the implant to avoid a metal overlap. The range of the design variations allow a projection of the gained results to "real" detectors. The most sensitive parameter for surface effects is the gap between the pixels which was adjusted by varying p–implantation widths at constant pitches from 10 μm to 100 μm. The pitch was varied like 1:2:4 from 50 μm to 200 μm and the length like 1:2:3 from 1000 μm to 3000 μm.

I-V measurements on the un-irradiated devices already show a significant contribution of the surface. Fig. 3 shows two exemplary I-V curves which have been measured on two individual pixels (1) with identical pitch and length but different gaps. The *wide–gap* design produces a higher current than the *small–gap* option. Because of identical pitch and length this difference is not due to volume effects but is caused by charge generation at the surface.

As expected from equation 2 the current difference should be proportional to the surface area. Characterising all different pixel designs on the test device we have analysed the total currents with respect to interface generation current. The interface generation current has been determined from the measured total pixel current by subtracting the volume generation current according to the volume generation current density measured on the large monitor diode. The interface generation current is plotted in fig. 4 versus the surface area surrounding the pixel where the surface area of a pixel cell is determined by the half gap distance on each side of the pixel and its length. As expected the additional current is proportional to the surface area. One important conclusion from this is that for

(1) For I-V measurements on single pixels the bias grid and the neighbouring pixels were grounded to avoid unwanted side effects as described in [10].

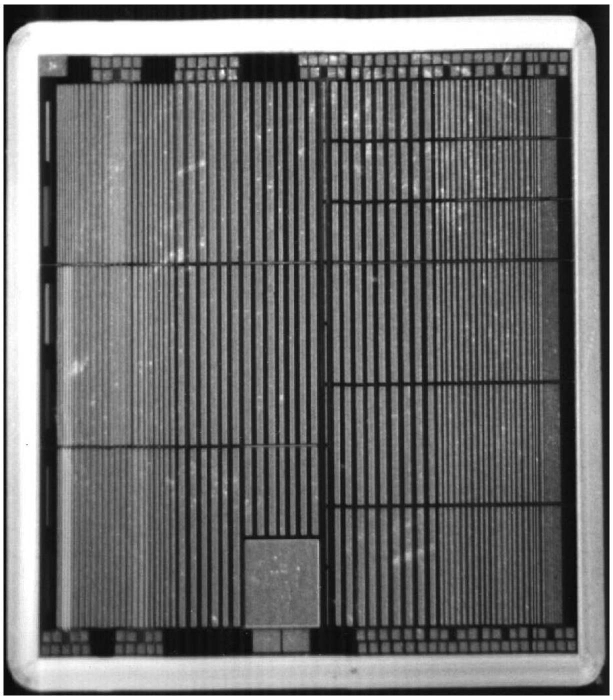

Fig. 2. – *Photo of the test device. The pixel lines are enclosed by a punch–through bias grid. A large monitor diode and two MOS capacitors can be seen at the bottom of the device. The active area is surrounded by a multi guard-ring structure.*

the un-irradiated device the whole surface area contributes to the total leakage current of a pixel cell and is completely depleted at high biases.

4. – Results after ionising radiation

All ionising particles produce surface damage when passing through silicon oxide. Depending on their energy they may also damage the silicon bulk, like protons or pions which are often used for irradiation tests. In this case it is difficult to distinguish between surface and bulk effects. To avoid those problems we have chosen a low energy electron beam (20 keV) generated with a modified electron microscope [11]. This technique allows to produce well controllable levels of surface damage. All irradiations have been performed without biasing the devices.

The irradiations have been performed in several dose steps, starting with 11 kGy and ending at an integral dose of 300 kGy. The I-V curves of different pixel designs were measured after all dose steps (after a defined annealing). Fig. 5 shows the curves after the low and the high dose for different designs. After both doses the current levels are as expected significantly higher than before irradiation. Neglecting the absolute current, the slope of the curves after both dose levels is similar. As before irradiation, pixels with wide gaps have higher leakage currents than those with smaller gaps. Additionally the I-V characteristics of the wide gap designs are dominated by an exponentially growing current while for the small gaps the current level remains constant. In case of the high dose the

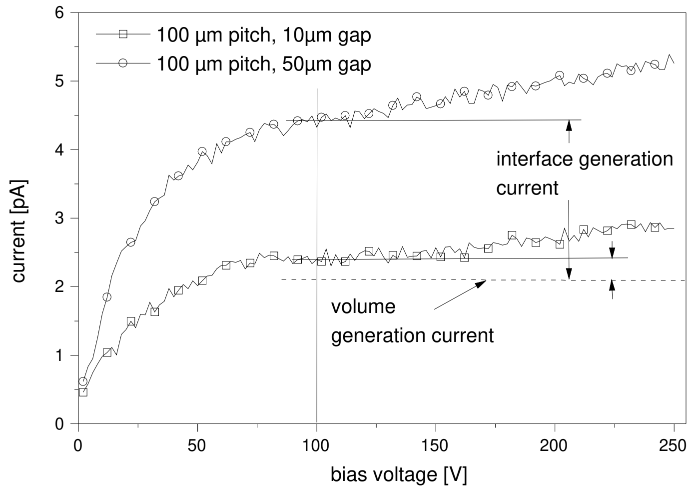

Fig. 3. – *Total leakage current vs. bias voltage measured on two pixels with identical pitch but different gaps.*

exponential increase is even more pronounced. Measurements after intermediate dose steps have confirmed the continuously increasing dominance of the exponential current fraction.

These observations can be explained as follows : the distribution of the positive oxide charges across the gap is sensitive to the potential distribution on the silicon oxide surface during irradiation. Potential distributions corresponding to *von Neumann* boundary conditions as well as to *gate* boundary conditions cause in-homogeneously distributed electrical fields. Generated by ionising particles, holes are trapped in the oxide near the interface and cause positive charge concentrations corresponding to the electrical field [12]. Therefore the flat–band voltage will vary across the gap between the pixels. When the depletion zones of the neighbour pixels connect by punch–through before the flat–band voltage is reached a fraction of the accumulated electrons are enclosed at the surface between the pixels. This region cannot be depleted even at higher bias voltages and contribute to the interface generation current. The electric field is peaking near the accumulation layers and electrical break downs occur.

The irradiations of our test devices have been done in a high vacuum environment and therefore the potential distribution on the oxide surface was comparable to von Neumann boundary conditions.

It was of interest to study how the I-V characteristics change with gate boundary conditions on the silicon oxide surface of an irradiated device. Therefore we have characterised the pixels of interest before and after adding an artificial gate contact with some silver loaded glue on the gap between them. This little trick enabled the comparison between both conditions on the same pixel. The corresponding I-V curves are shown in fig. 6 for both designs.

Looking at the wide gap result in fig. 6a, the difference in the curves is obvious. The gate contact stabilises the pixel current, there is no exponential behaviour observable. Fig. 7 shows a cutting of the I-V curve together with a C-V measurement performed on the same pixel. The two measurements show the correlation of the flat–band voltage and

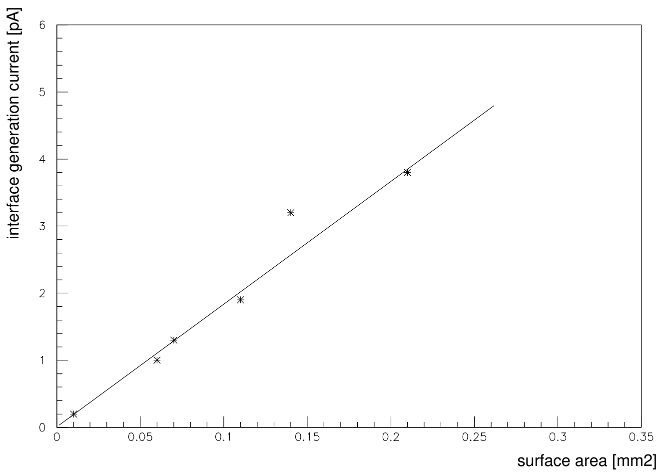

Fig. 4. – *Measured interface generation current versus surface area.*

the current step, which is due to interface generation current.

In case of the small gap design there is no significant change in the I-V characteristic by the gate contact visible. At higher voltages a slightly exponential increase is measured under both conditions. Taking the normalised interface generation current of the wide gap cells it is possible to predict the interface current for the other design which is two times higher than the measured value. This indicates that only a fraction of the surface is depleted and contributes. An enclosed accumulation layer is present, even in case of high bias voltages, whereas in case of the wide gap design all the surface is depleted.

As reported in [13], a similar effect was observed from two dimensional device simulations assuming gate boundary conditions.

5. – Conclusions

After ionising radiation the I-V curves of single pixels show an exponential current increase. This effect is more pronounced on wide gap (100 μm) designs than on small gap (10 μm) options and is caused by enclosed electron accumulation layers in the gap between the pixels.

When applying gate boundary conditions, which can be achieved by a high–ohmic passivation layer like nitride on the oxide, to the oxide surface the leakage current of the wide gap pixel cells is dominated by interface generation current. The whole surface is depleted. In case of small gaps an enclosed electron layer is still present because a punch–through of the depleted regions occurs before the flat–band voltage is reached.

Although the I-V curves have indicated the enclosure of accumulated electrons for the small gap design, it is not possible to deduce any information about the electrical field distribution or the position of the electron accumulation from them. It is planned for the future to use a scanning proton micro beam to measure the position of the enclosed electron accumulation as reported in [14] and to extend the studies to the impact of bias

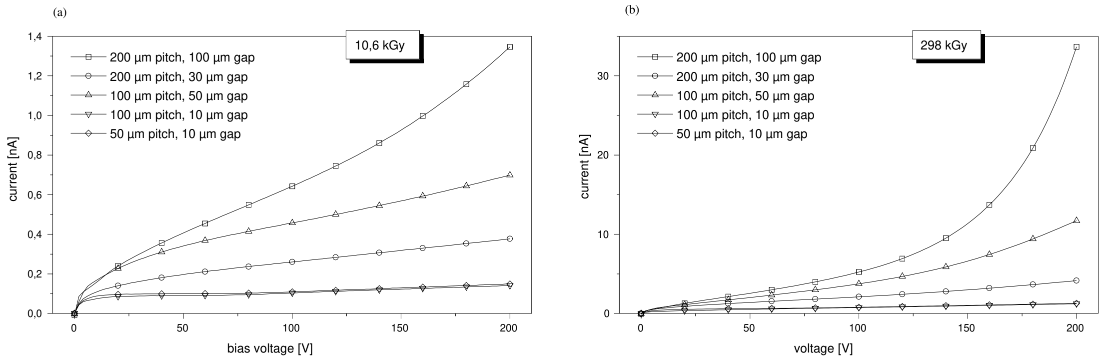

Fig. 5. – *IV characteristics of several pixel designs after (a) 11 kGy and (b) 300 kGy.*

voltages on surface effects.

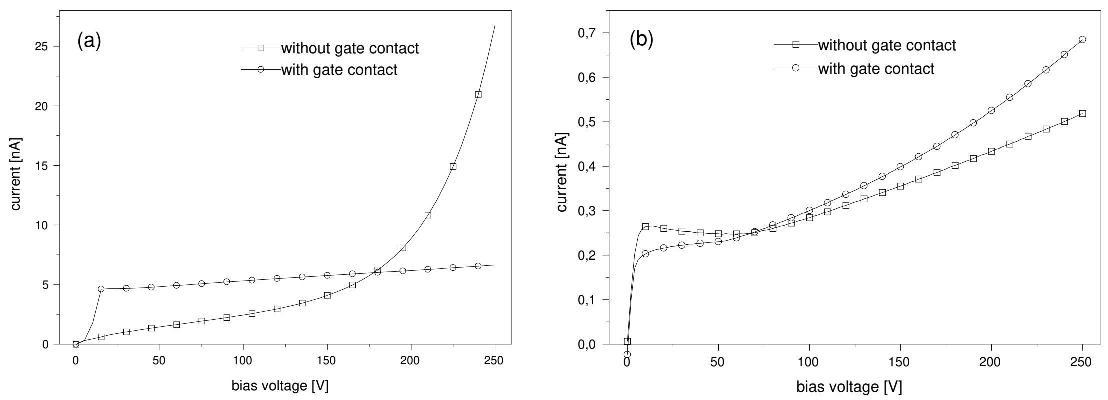

Fig. 6. – *IV measurements after 11 kGy of (a) 100 μm gap pixels and (b) 10 μm gap pixels. Both pixels have been characterised with and without gate contact in the gap.*

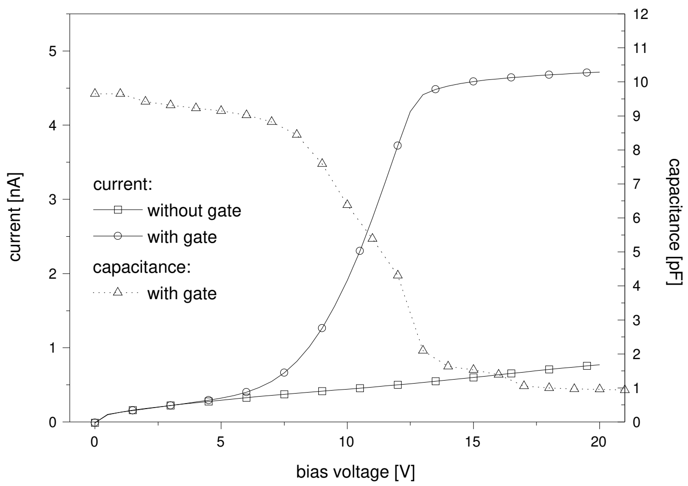

Fig. 7. – *Excerpt of fig. 6 (a) together with a C-V measurement of the same pixel.*

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